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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/751,551	12/28/2000	Jingyu Lian	00 P 9119 US	9195

7590 06/14/2002
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DALLAS, TX 75252-5793

EXAMINER

ORTIZ, EDGARDO

ART UNIT	PAPER NUMBER
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2815

DATE MAILED: 06/14/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

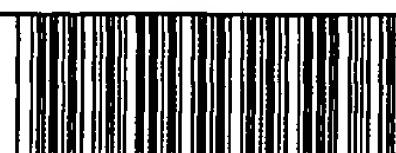
Office Action Summary

Application No.
09/751,551

Applicant(s)
Lian Et.al.

Examiner
Edgardo Ortiz

Art Unit
2815



-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on February 27, 2002 and March 25, 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 and 21-24 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 21-24 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
*See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 1 1/2 6) ☐ Other:

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DETAILED ACTION

This Office Action is in response to an amendment filed February 27, 2002 and the supplemental amendment filed on March 25, 2002, on which Applicant added new claims 21-24.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 8, 22 and 24 are rejected under 35 U.S.C. § 102 (b) as being anticipated by Applicant's admitted prior art, as shown on figure 2. With regard to Claim 8, Applicant's admitted prior art teaches a conductive barrier layer (122), a first conductive liner (132) deposited over the conductive barrier layer and a second conductive liner (134) deposited over the first conductive liner, the second conductive liner comprising a conductive oxide and a conductive layer (124) deposited on the second conductive liner.

With regard to Claim 22, Applicant's admitted prior art teaches a second conductive liner (134) that comprise IrO₂ or RuO₂.

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With regard to Claim 24, Applicant's admitted prior art teaches both a conductive layer (124) and a first conductive liner (132) that comprise Pt, Ir, Ru, Pd or combinations thereof.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-7, 9-13, 21 and 23 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Applicant's admitted prior art, as shown in figure 2 in view of Kotecki (BaSrTiO₃ dielectrics for future stacked-capacitor DRAM). With regard to Claim 1, Applicant's admitted prior art teaches a conductive barrier layer (122), a first conductive liner (132) deposited over the conductive barrier layer and a second conductive liner (134) deposited over the first conductive liner, the second conductive liner comprising a conductive oxide and a conductive layer (124) deposited on the second conductive liner.

However, Applicant's admitted prior art fails to teach that the conductive layer and the first conductive liner comprise the same material. Kotecki teaches a DRAM structure which includes a conductive barrier layer (TaSiN), a first conductive liner (Pt), a dielectric layer (BSTO) and a

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conductive layer (Pt) deposited over the dielectric layer, wherein the conductive layer and the first conductive liner comprise the same material, in this case Pt. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include a conductive layer and a first conductive liner comprising the same material, as clearly suggested by Kotecki, in order to provide electrodes with good adhesion and electrical conductivity characteristics.

With regard to Claim 2, Applicant's admitted prior art teaches a layer (134) including second conductive liner that comprise a conductive oxide (IrO_2).

With regard to Claims 3, 5, 9 and 11; a further difference between the claimed invention and Applicant's admitted prior art is, the thicknesses of the first and second conductive liners. It would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include the thickness of the first and second conductive liners as claimed, in order to reduce oxygen diffusion into a conductive layer such as polysilicon below the multi-layer electrode.

With regard to Claims 4 and 10, a further difference between the claimed invention and Applicant's admitted prior art is, the conductive layer and the first conductive liner comprising Pt. Kotecki teaches a DRAM structure which includes a conductive barrier layer (TaSiN), a first

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conductive liner (Pt), a dielectric layer (BSTO) and a conductive layer (Pt) deposited over the dielectric layer, wherein the conductive layer and the first conductive liner comprise the same material, in this case Pt. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include a conductive layer and a first conductive liner comprising Pt, as clearly suggested by Kotecki, in order to provide electrodes comprising Pt which has good adhesion and electrical conductivity characteristics.

With regard to Claims 6 and 12, a further difference between Applicant's admitted prior art and the claimed invention is, a conductive barrier layer that comprises TaSiN. Kotecki teaches a conductive layer that comprises TaSiN. Therefore, it would have been an obvious modification to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Applicant's admitted prior art to include a conductive barrier layer that comprises TaSiN, as clearly suggested by Kotecki, since it is a well known barrier layer material because of its oxidation preventing quality.

With regard to Claims 7 and 13, a further difference between Applicant's admitted prior art and the claimed invention is, an integrated circuit that comprises a DRAM or a FRAM. Kotecki teaches a DRAM structure which includes a conductive barrier layer (TaSiN), a first conductive liner (Pt), a dielectric layer (BSTO) and a conductive layer (Pt) deposited over the dielectric layer.

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Therefore, it would have been obvious to someone with ordinary skill in the art, at the time of the invention, to use a multi-layer electrode structure as the one disclosed by Kotecki in a memory device such as a FRAM or DRAM.

With regard to Claim 21, Applicant's admitted prior art teaches a second conductive liner (134) that comprise IrO₂ or RuO₂.

With regard to Claim 23, Applicant's admitted prior art teaches both a conductive layer (124) and a first conductive liner (132) that comprise Pt, Ir, Ru, Pd or combinations thereof.

Response to Arguments

3. Applicant's arguments with respect to claims 1-13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Edgardo Ortiz (Art Unit 2815), whose telephone number is (703) 308-6183 or by fax at (703) 308-7722. In case the Examiner can not be reached, you might call Supervisor Eddie Lee at (703) 308-1690. Any inquiry of a general nature or relating to the status

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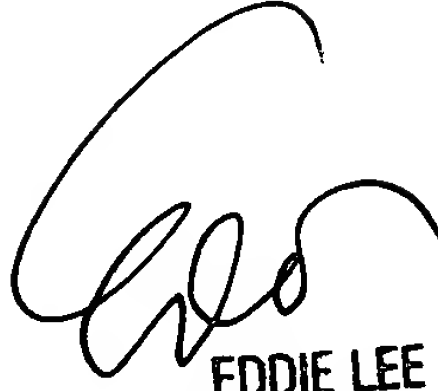
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of this application should be directed to the Group 2800 receptionist whose telephone number is
(703) 308-0956.

EO/AU 2815

6/12/02



EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800